Please amend the specification as follows:

On pages 3-4 of the specification, please replace the following paragraphs:

In order to overcome this problem, memory chip 300 is enhanced by adding an SRAM bank (310SRAM), featuring a dual port function that allows receiving and transferring data within a clock cycle. The access operation of the DRAM banks (310DRAM) and SRAM (310SRAM) are controlled by the TAG memory (310TAG), while the memory access of the memory chip 300 is enabled by a read or write command (not shown), a bank address (XBADD), and a word address (XWADD), wherein XBADD and XWADD identify one of the DRAM banks (310DRAM) and the appropriate wordline within the selected DRAM banks. When the memory access is enabled, wordline (320TAG) in the TAG memory (310TAG) and the wordlines (320s) in SRAM bank (310SRAM) are activated by decoding the word address (XWADD). This enables reading out data in the memory cells (330TAG) in within the TAG memory (310TAG) and data in the memory cells (330s) within the SRAM buffer (310SRAM). The read data bits (330TAG) of the TAG memory (310TAG) defines the bank address (TBADD) which, in turn, identifies the corresponding DRAM bank for the data bits (330s) currently read from the SRAM buffer (310SRAM). When TBADD coincides with the bank address input (XBADD), the data bits (330s) are the ones that are requested by the memory access command, since the data bits (330s) were previously copied from the corresponding DRAM bank to the SRAM buffer (310SRAM). Therefore, no DRAM bank access is necessary, and the read data bits from the SRAM ~~SARM~~ buffer (310SRAM) are read out from the XDATA pins. On the other hand, if TBADD differs from the bank address inputs (XBADD), the TAG memory (310TAG) control the DRAM banks (310DRAM) as follows.

Assuming that TBADD ~~TADD~~ identifies DRAM bank (310i), then, the data bits (330s) in the SRAM buffer (310SRAM) are stored back in DRAM bank (310i), where the wordline 320i is same as the wordline address of 320s (Direct Mapping). This allows data bits to be transferred from the SRAM memory cells (330s) to the DRAM memory cells (330i). Concurrent with the bank address input (XBADD), the corresponding DRAM bank (310j) is activated for a read operation. Then, the cell's data bits (330j) in the corresponding DRAM bank (310j) are read out, where wordline 320j coincides with the wordline address of 320s (Direct Mapping). They are read out from the XDATA pins. The cell's data bits (330j) are also stored in the cells (330s) of

the SRAM buffer (310SRAM). TBADD is therefore updated to identify the DRAM bank 310j for a future memory access command. For a subsequent same addressing pattern (i.e., 330j), data bits are read out or written into the SRAM buffer (310SRAM), enabling a refresh operation of the memory cells even when only one array (i.e., 330j) is continuously addressed. This is possible since, eventually, the data bits in the array will be copied to the SRAM array, refreshing the array without infringing on any violations.

On page 5 of the specification, please replace the following paragraph:

It is another object of the invention to provide a concurrent refresh operation to an embedded DRAM without resorting to using ~~a SARM~~ an SRAM buffer.

On page 7 of the specification, please replace the following paragraph:

Fig. 2 shows a block diagram representing a multi-bank DRAM memory device to illustrate how the memory availability improves by ~~a~~ applying a prior art concurrent performance of a refresh operation while enabling the memory access.